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Regulating Pulse Width Modulator

FEATURES

- *Guaranteed* ±2% Reference Tolerance
- *Guaranteed* ±6% Oscillator Tolerance
- *Guaranteed* 10mV/1000 Hrs Long Term Stability
- Interchangeable with all SG1524 or LM1524 Devices
- Operates Above 100kHz

APPLICATIONS

- Switching Power Supplies
- Motor Speed Control
- Off-Line Power Converters

Jameco part Number 31974

DESCRIPTION

The LT1524 PWM switching regulator control circuit contains all the essential circuitry to implement single-ended or push-pull switching regulators. Included on the circuit are oscillator, voltage reference, a pulse width modulator, error amplifier, overload protection circuitry and output drivers.

Although pin-for-pin and functionally compatible with industry standard 1524 and 3524 devices, Linear Technology has incorporated several improvements in the design of the LT1524. A subsurface zener reference has been used to provide excellent stability with time and the reference is trimmed at the wafer level to provide an initial accuracy of 2%. Additionally, the oscillator is trimmed to provide a maximum tolerance of 6%.

Linear Technology Corporation's advanced processing, design and passivation techniques make the LT1524 and LT3524 a superior and more reliable choice over previous devices.

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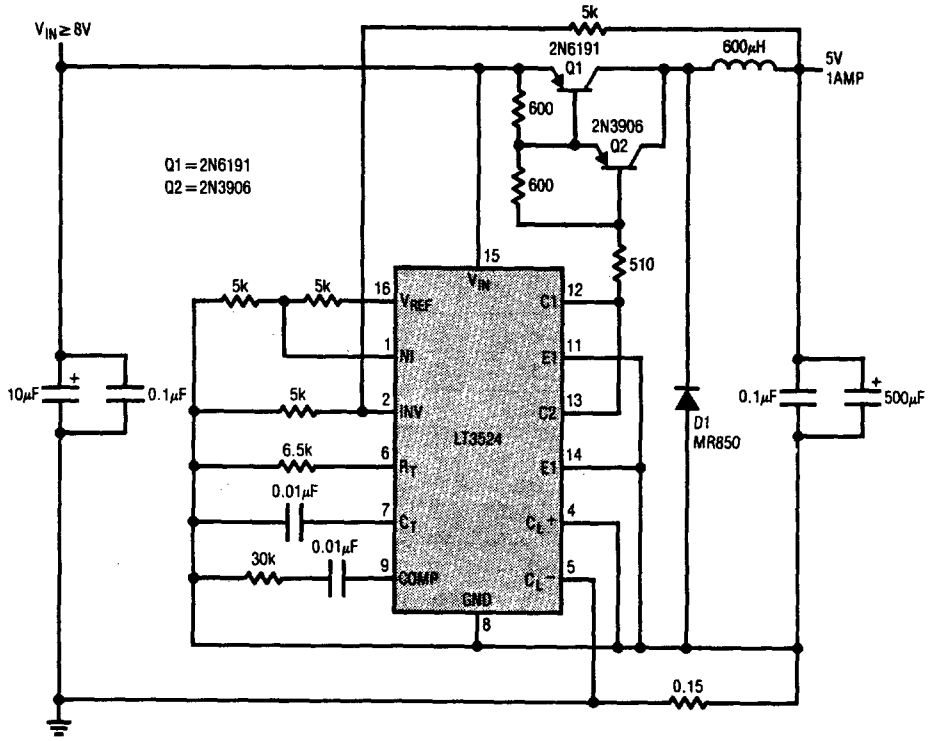
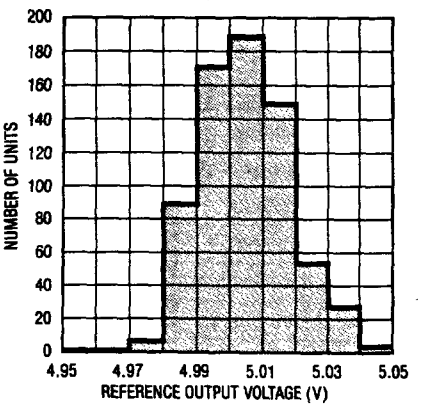
5V, 1 Amp Regulator



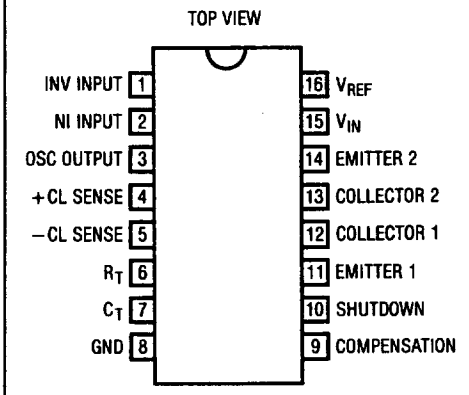
Distribution of Reference Output Voltage



ABSOLUTE MAXIMUM RATINGS

Input Voltage 40V
Reference Output Current 50mA
Output Current (Each Output) 100mA
Oscillator Charging Current (Pin 6 or 7) 5mA
Internal Power Dissipation (Note 1) 1W
Operating Temperature Range
LT1524/SG1524 ..... −55°C to +125°C
LT3524/SG3524 ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

PACKAGE/ORDER INFORMATION



J PACKAGE
16 PIN HERMETIC

N PACKAGE
16 PIN PLASTIC

ORDER PART NUMBER
LT1524J
LT3524J
LT3524N
SG1524J
SG3524J
SG3524N

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		LT1524 MIN	LT1524 TYP	LT1524 MAX	SG1524 MIN	SG1524 TYP	SG1524 MAX	UNITS
Reference Section:									
Output Voltage		●	4.9	5.0	5.1	4.8	5.0	5.2	V
Line Regulation	V_{IN} = 8V to 40V	●		2	10		10	20	mV
Load Regulation	I_L = 0mA to 20mA	●		10	20		20	50	mV
Ripple Rejection	f = 120Hz			80			66		dB
Short Circuit Current Limit	V_{REF} = 0			100			100		mA
Temperature Stability		●		0.3	1		0.3	1	%
Long Term Stability				2	10		20		mV/khr
Oscillator Section:									
Maximum Frequency	C_T = 0.001μF, R_T = 2kΩ	●		300			300		kHz
Initial Accuracy	R_T and C_T Constant			3	6		5		%
Voltage Stability	V_{IN} = 8V to 40V				1			1	%
Temperature Stability	Note 3	●		2			2		%
Output Amplitude	Pin 3			3.5			3.5		V
Output Pulse Width	C_T = 0.01μF, T_A = 25°C			0.5			0.5		μs
Error Amplifier Section:									
Input Offset Voltage	V_{CM} = 2.5V	●		0.5	5		0.5	5	mV
Input Bias Current	V_{CM} = 2.5V	●		0.5	2		2	10	μA
Open Loop Voltage Gain		●	72	80		72	80		dB
Common-Mode Voltage		●	1.8		3.4	1.8		3.4	V
Common-Mode Rejection Ratio			70	86			70		dB
Small Signal Bandwidth	A_V = 0dB			3			3		MHz
Output Voltage			0.5		3.8	0.5		3.8	V

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT1524 MIN	LT1524 TYP	LT1524 MAX	SG1524 MIN	SG1524 TYP	SG1524 MAX	UNITS
Comparator Section:									
Minimum Duty Cycle		●			0			0	%
Maximum Duty Cycle		●	45	49		45	49		%
Input Threshold	Zero Duty Cycle	●		1			1		V
Input Threshold	Max Duty Cycle	●		3.5			3.5		V
Input Bias Current		●		0.2	2		1		µA
Current Limiting Section:									
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max Out		190	200	210	190	200	210	mV
Sense Voltage T.C.		●		0.2			0.2		mV/°C
Common-Mode Voltage		●	−0.7		1	−0.7		1	V
Output Section: (Each Output)									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	V_{CE} = 40V	●		0.1	50		0.1	50	µA
Saturation Voltage	I_C = 50mA	●		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	●	17	18		17	18		V
Rise Time	R_C = 2kΩ			0.2			0.2		µs
Fall Time	R_C = 2kΩ			0.1			0.1		µs
Total Standby Current:	V_{IN} = 40V (Note 4)	●		8	10		8	10	mA

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS		LT3524 MIN	LT3524 TYP	LT3524 MAX	SG3524 MIN	SG3524 TYP	SG3524 MAX	UNITS
Reference Section:									
Output Voltage		●	4.9	5.0	5.1	4.6	5.0	5.4	V
Line Regulation	V_{IN} = 8V to 40V	●		3	10		10	30	mV
Load Regulation	I_L = 0mA to 20mA	●		10	20		20	50	mV
Ripple Rejection	f = 120Hz			80			66		dB
Short Circuit Current Limit	V_{REF} = 0			100			100		mA
Temperature Stability		●		0.3	1		0.3	1	%
Long Term Stability				2	10		20		mV/khr
Oscillator Section:									
Maximum Frequency	C_T = 0.001µF, R_T = 2kΩ	●		300			300		kHz
Initial Accuracy	R_T and C_T Constant			3	6		5		%
Voltage Stability	V_{IN} = 8V to 40V				1			1	%
Temperature Stability	Note 3	●		2			2		%
Output Amplitude	Pin 3			3.5			3.5		V
Output Pulse Width	C_T = 0.01µF, T_A = 25°C			0.5			0.5		µs
Error Amplifier Section:									
Input Offset Voltage	V_{CM} = 2.5V	●		1	5		2	10	mV
Input Bias Current	V_{CM} = 2.5V	●		0.5	2		2	10	µA
Open Loop Voltage Gain		●	72	80		60	80		dB
Common-Mode Voltage			1.8		3.4	1.8		3.4	V
Common-Mode Rejection Ratio			70	86			70		dB
Small Signal Bandwidth	A_V = 0dB			3			3		MHz
Output Voltage			0.5		3.8	0.5		3.8	V

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ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS		LT3524 MIN	LT3524 TYP	LT3524 MAX	SG3524 MIN	SG3524 TYP	SG3524 MAX	UNITS
Comparator Section:									
Minimum Duty Cycle		●			0			0	%
Maximum Duty Cycle		●	45	49		45	49		%
Input Threshold	Zero Duty Cycle	●		1			1		V
Input Threshold	Max Duty Cycle	●		3.5			3.5		V
Input Bias Current		●		1	2		1		μA
Current Limiting Section:									
Sense Voltage	Pin 9 = 2V with Error Amplifier Set for Max Out		190	200	210	180	200	220	mV
Sense Voltage T.C.		●		0.2			0.2		mV/°C
Common-Mode Voltage		●	−1		1	−1		1	V
Output Section: (Each Output)									
Collector-Emitter Voltage		●	40			40			V
Collector Leakage Current	V_{CE} = 40V	●		0.1	50		0.1	50	μA
Saturation Voltage	I_C = 50mA	●		1	2		1	2	V
Emitter Output Voltage	V_{IN} = 20V	●	17	18		17	18		V
Rise Time	R_C = 2kΩ			0.2			0.2		μs
Fall Time	R_C = 2kΩ			0.1			0.1		μs
Total Standby Current:	V_{IN} = 40V (Note 4)	●		8	10		8	10	mA

The ● denotes specifications that apply over the full operating temperature range.

The shaded electrical specifications indicate those parameters which have been improved or guaranteed test limits provided for the first time.

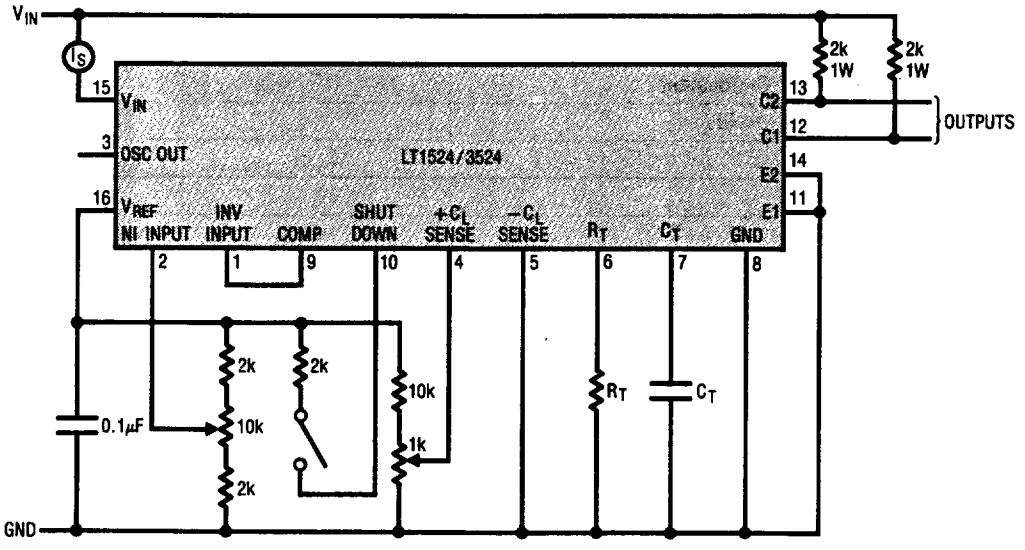
Note 1: For operating at elevated temperatures, the device in the J package must be derated at 100°C/W to a maximum junction temperature of 150°C, while the device in the N package is derated at 150°C/W to a maximum junction temperature of 115°C.

Note 2: These specifications apply for V_{IN} = 20V, f = 20kHz. T_A = 25°C unless otherwise noted.

Note 3: Although many manufacturers specify a maximum specification of 2%, Linear Technology's experience is that this specification is not being presently met by other manufacturers. Linear Technology's basic design, although improved, is essentially identical to other manufacturers' devices. Linear Technology is, however, unwilling to place a maximum specification on its data sheet which cannot be met or guaranteed.

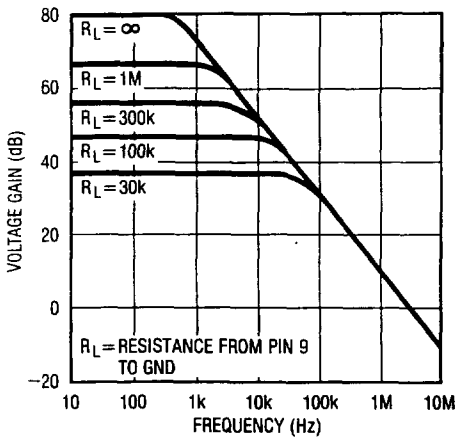
Note 4: Standby current does not include the oscillator charging current, error and current limit dividers, and the outputs are open circuit.

TEST CIRCUIT

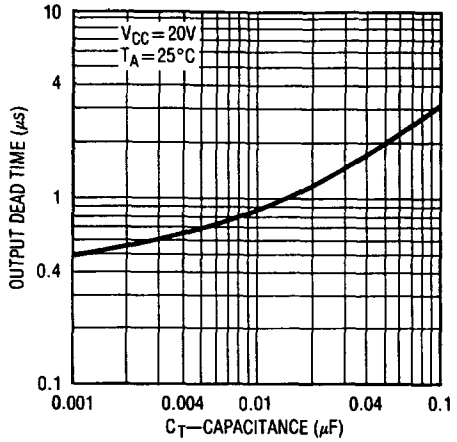


TYPICAL PERFORMANCE CHARACTERISTICS

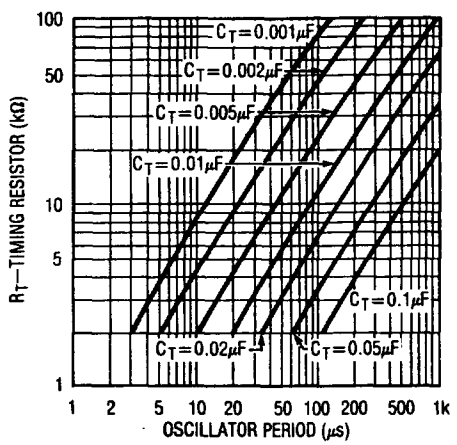
Error Amplifier Gain



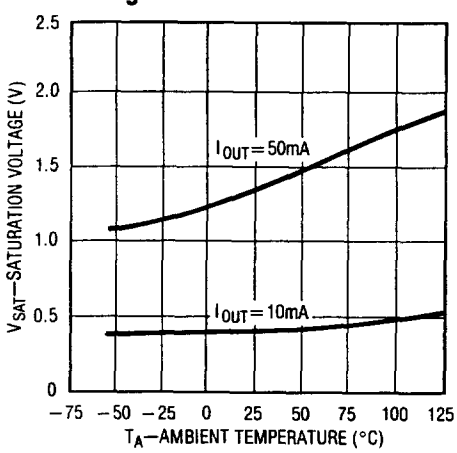
Output Dead Time



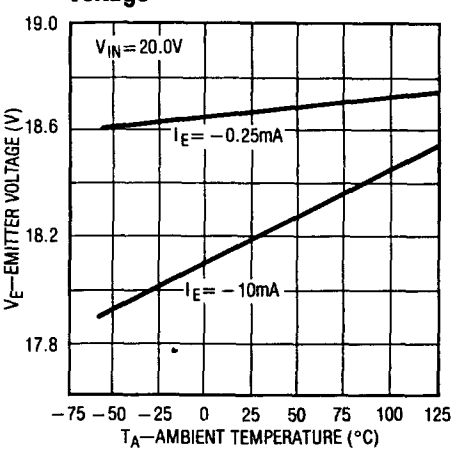
Oscillator Period



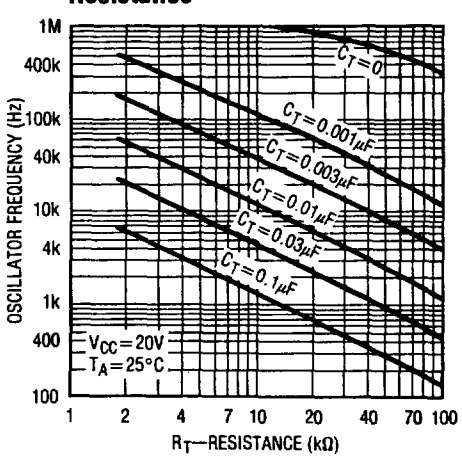
Output Transistor Saturation Voltage



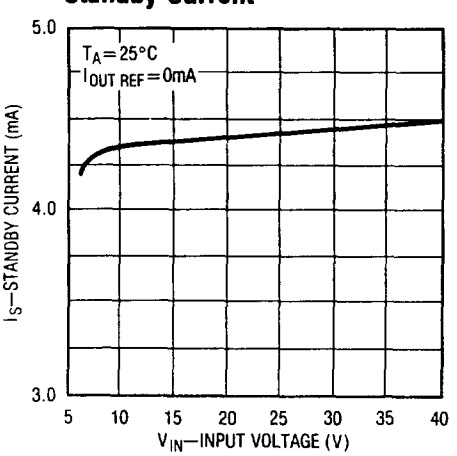
Output Transistor Emitter Voltage



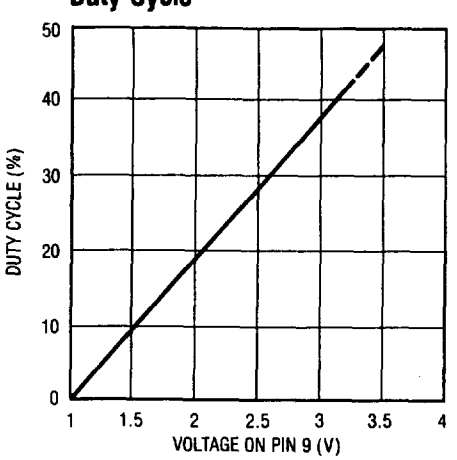
Oscillator Frequency vs Timing Resistance



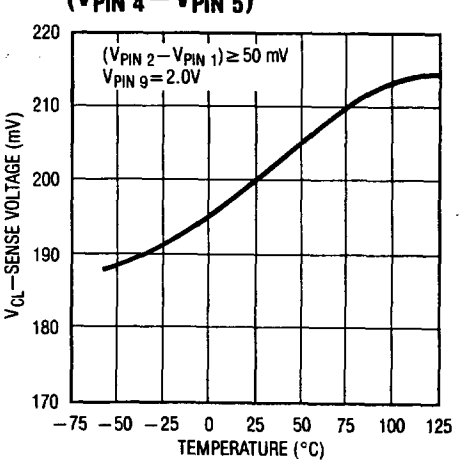
Standby Current



Duty Cycle



Current Limit Sense Voltage ($V_{PIN\ 4} - V_{PIN\ 5}$)



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APPLICATIONS INFORMATION

FUNCTIONAL DESCRIPTION AND PIN FUNCTIONS

Voltage Regulator

The internal 5V regulator (input pin 15, output pin 16) supplies a regulated 5V to all internal circuitry, as well as up to 50mA for external circuitry. For operation below 8V input, pins 15 and 16 may be tied together and 5V to 6V externally applied.

Oscillator

The internal oscillator circuitry sets the frequency of operation for the switching regulator. The oscillator waveform is a ramp from about 1V to 3.5V (pin 7). Frequency is set by a timing resistor from pin 6 to ground and a capacitor from pin 7 to ground. The oscillator period is approximately RC for the recommended range of 1.8k to 100k for R and 0.001μF to 0.1μF for C.

The fall time of the ramp sets the blanking or dead time where both outputs are off in push-pull regulators. This is controlled by the value of the capacitor alone.

Output Transistors

The two output transistors have both the emitters (pins 11 and 14) and the collectors available (pins 12 and 13). Internal current limiting for both of these transistors is about 100mA. The two transistors are driven 180° out of phase by the flip-flop. For single-ended operation they should be connected in parallel.

Error Amplifier

The differential input (pins 1 and 2) single-ended output (pin 9) transconductance amplifier provides about 80dB of gain, as well as providing a point for loop frequency compensation or electronic shutdown.

DC gain of the loop can be controlled by resistive loading, while AC compensation is usually accomplished with a series R-C connected from pin 9 to ground. The output impedance at pin 9 is about 5MΩ and current is about 200μA, so external op-amps or voltage sources can easily drive the comparator input. Normally, the 5V reference is divided down to generate a voltage within the common-mode range of the error amplifier.

Synchronous Operation

When an external clock is desired, a clock pulse of approximately 3V can be applied directly to the oscillator output, pin 3. The impedance to ground at this point is approximately 2kΩ. In this configuration, R_T C_T must be selected for a clock period slightly greater than that of the external clock.

If two or more LT1524 regulators are to be operated synchronously, all oscillator output terminals should be tied together. The oscillator programmed for the minimum clock period will be the master from which all the other LT1524s operate. In this application, the C_T R_T values of the slaved regulators must be set for a period approximately 10% longer than that of the master regulator. In addition, C_T (master) = 2 C_T (slave) to ensure that the master output pulse, which occurs first, has a wider pulse width and will subsequently reset the slave regulators.

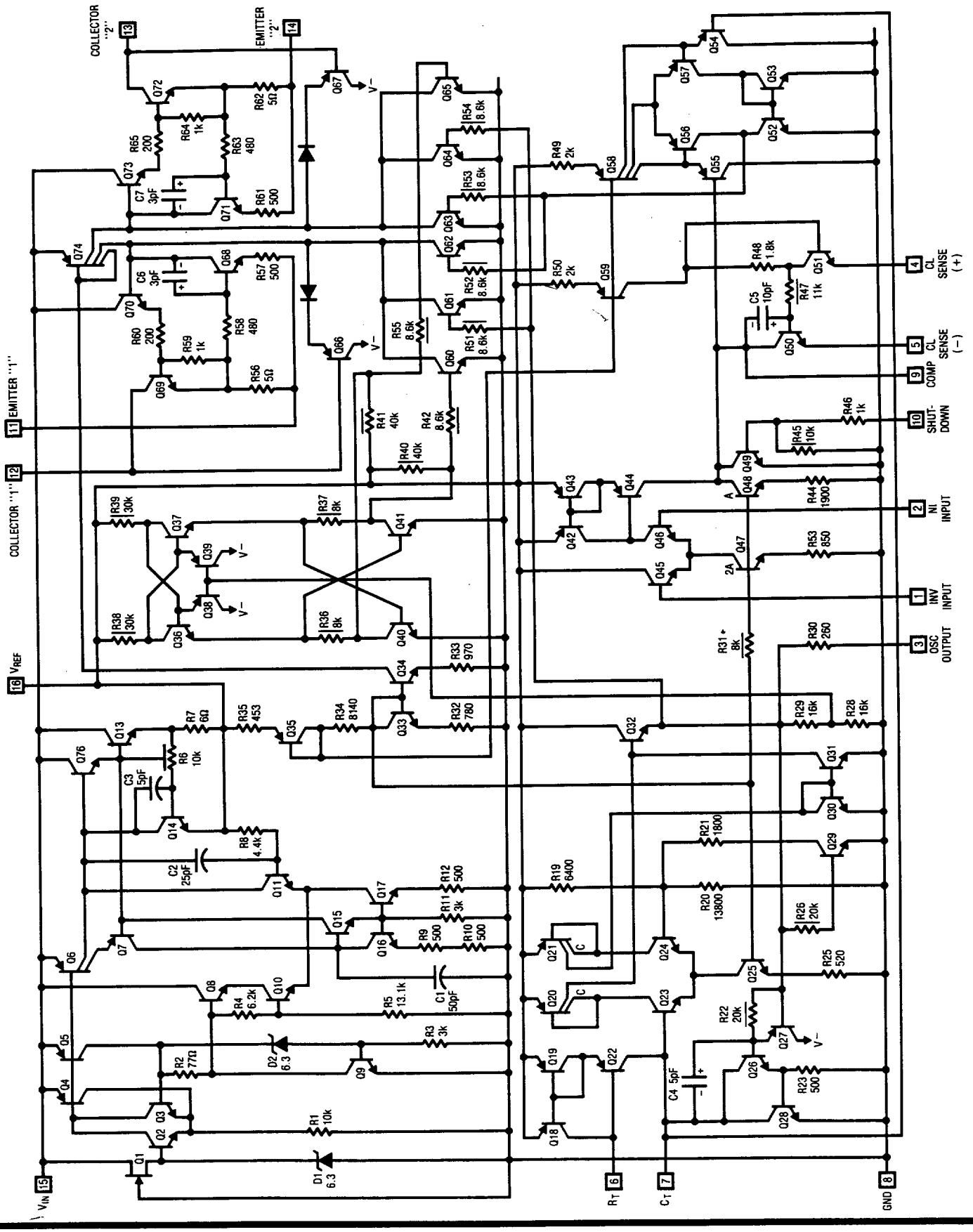
Shutdown

A logic high at pin 10 will shut down the regulator and cause both output transistors to turn off.

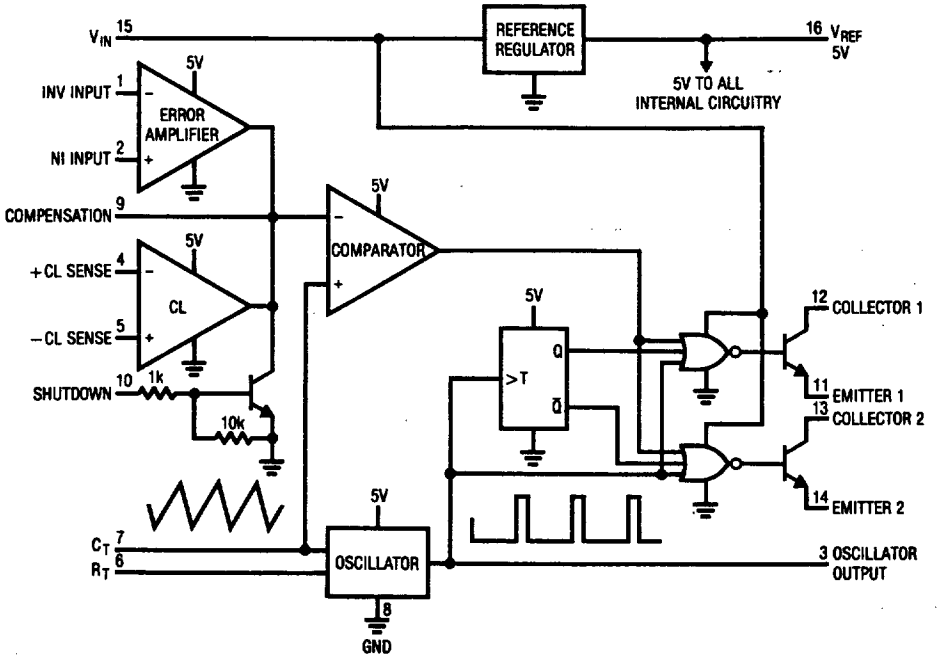
Current Limit

Current limiting is activated when the voltage between pins 4 and 5 exceeds 200mV. The output of the current limit amplifier internally sums with the error amplifier to shorten the output pulse width. The gain of the current limit circuitry is relatively low, so current control in limit is typically about 5%. Two areas of caution should be observed with current limiting. First, the response time of the current limit is set by the loop roll-off on pin 9. Fast current limiting requires external circuitry. Second, the common-mode range of the current limit amplifier is limited. Even fast spikes outside this range can disrupt operation.

SCHEMATIC DIAGRAM



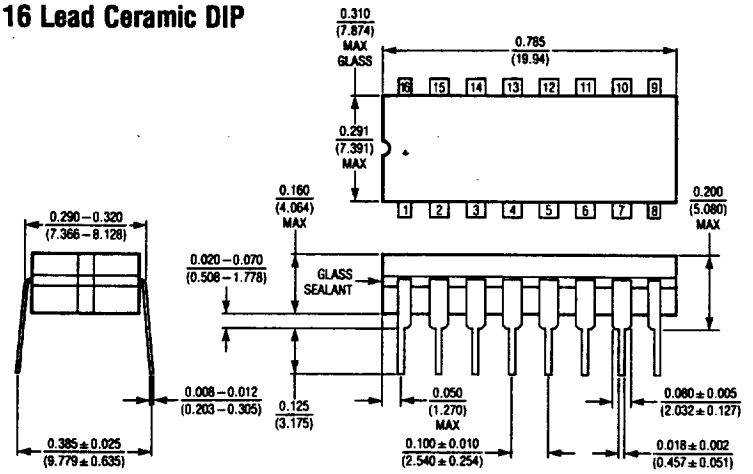
BLOCK DIAGRAM



PACKAGE DESCRIPTION

J Package
16 Lead Ceramic DIP

	T_J MAX	Θ_{JA}	Θ_{JC}
LT1524J SG1524J	150°C	100°C/W	30°C/W
LT3524J SG3524J	150°C	100°C/W	30°C/W



N Package
16 Lead Plastic DIP

	T_J MAX	Θ_{JA}	Θ_{JC}
LT3524N SG3524N	115°C	140°C/W	50°C/W